In the Drawings

Figure 1 Change "MP" in reference number 12 to "MPU."

Figure 15 Change lower reference number "140" to "142."

REMARKS

The claims are claims 1, 6 to 11 and 16 to 20.

The application has been further amended at many locations to correct minor errors and to present uniform language throughout. The amendments include correction of those errors noted by the Examiner and an update of the status of the co-pending application cited at page 1.

Two new drawing sheets incorporating drawing corrections required by the Examiner are attached.

Claims 1 and 11 are amended. Claims 2 to 5 and 12 to 15 are canceled. Claims 1 and 11 are amended to include subject matter disclosed in the original application at page 18, line 25 to page 19, line 8.

Claims 1 to 22 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner states the term "control word" is indefinite because it neither clearly states it corresponds to a bus width or a fixed bit length nor states it is to be considered a varying bit length.

This rejection is cured by reference to "task attribute bits" a term also used in the original application. The Applicants respectfully submit that one skilled in the art would clearly recognize that this term is confined to no fixed length but can vary with the needs of a particular application. As such this refers to a collection of bits as the Examiner construed "control word" in examining this application.

The Examiner further rejected claims 14 and 15 because the recitation "said enabling or disabling" had no antecedence. This rejection is cured by cancellation of claims 14 and 15.

Claims 1 to 22 were provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-26 of copending U.S. Patent Application Serial No. 09/932,354. The Examiner notes the application No. 09/932,354 recites "configured" and this application recites "selectively enabled and disabled." The Examiner states that "may be selectively configured" is in fact the same as a "may be selectively enabled and disabled."

Claims 1 and 11 have been amended to recite subject matter not claimed in U.S. Patent Application Serial No. 09/932,354. As amended claims 1 and 11 recite a logical OR operation taught at page 18, line 25 to page 19, line 8 of this application. This logical OR operation is not claimed in U.S. Patent Application Serial No. 09/932,354. Accordingly, the provisional double patenting reject should be withdrawn.

Claims 1 to 22 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Gouzu et al. EP 0 794 481 A2, Gasztonyi U.S. Patent No. 5,339,445, Shaffer et al. U.S. Patent No. 6,298,448 and Gupta et al. U.S. Patent No. 5,996,083.

Claims 1 and 11 recite subject matter not made obvious by the combination of Gouzu et al, Gasztonyi, Shaffer et al and Gupta et al. Claim 1 recites "a logical OR gate having inputs receiving a bit of each the task attribute register corresponding to the at least one associated circuit used by more than one task and an output connected to the power input of the associated circuit used by more than one task to enable the associated circuit used by more than one task when task using the associated circuit is being executed by the processing module and to disable the associated circuit used by more than one task when no task using the associated circuit is being executed by the processing module." Similarly, claim 11 recites "logical ORing task attribute bits of said more than one task corresponding to said at least one associated circuit used by more than one task to enable said

associated circuit used by more than one task when any task using said associated circuit is being executed by the processing module and to disable said associated circuit when no task using said associated circuit is being executed by the processing module." The recitation of the OR operation is not made obvious by the combination cited by the Examiner. First, Gouzu and Shaffer et al teach only clock rate control and fail to teach the selective powering recited in claims 1 and 11. Gasztonyi does not teach that power management 46 forms the recited OR operation nor controls the powering of an associated circuit based upon such an OR operation. Gupta et al does not teach the claimed OR operation. Gupta et al states at column 8, lines 2 to 5:

> "Where the power control register field is multiple bits, however, the logic 160 will be combinational logic that will decode the predetermined value and will deassert the enable signal when that value is detected."

This teaching of "combinational logic" fails to make obvious the recited OR operation. Particularly, the combinational logic taught in Gupta et al fails to state that the OR is of bits of differing task attribute bits as recited in claims 1 and 11. Accordingly, claims 1 and 11 are allowable over the combination of Gouzu et al, Gasztonyi, Shaffer et al and Gupta et al.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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